WHAT WE CLAIM ARE:

1. A method of manufacturing a semiconductor device comprising steps of:

(a) forming a first interlayer insulating film made of insulating material on a semiconductor substrate having semiconductor elements formed on a surface of the substrate;

(b) forming a first intra-layer insulating film made of insulating material on the first interlayer insulating film;

(c) forming a recess through the first intra-layer insulating film, wherein the recess has a pad part and a wiring part continuous with the pad part, the pad part has a width wider than a width of the wiring part, a plurality of convex regions are left in the pad part, and the recess is formed so that the convex regions are disposed in such a manner that a recess area ratio in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than a recess area ratio in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width;

(d) forming a first film made of conductive material on the semiconductor substrate, the first film being filled in the recess; and

(e) removing an upper region of the first film to form a first pad made of the first film left in the recess.

2. A method according to claim 1, further comprising steps of, after the step (e):

(f) forming a second interlayer insulating film made of insulating material on the first intra-layer insulating film and the left first film;

(g) forming at least one via hole through the second interlayer

insulating film, the via hole being included in the first pad as viewed along a direction parallel to a substrate normal; and

(h) forming a second pad on the second interlayer insulating film, the second pad being connected to the first pad via a region in the via hole.

3. A method according to claim 2, further comprising a step of, after the step (h):

(i) inspecting the semiconductor elements by making a conductive probe in contact with the second pad.

4. A method according to claim 3, further comprising a step of, after the step (i):

(j) scribing the semiconductor substrate along a line inside the second pad.

5. A method according to claim 1, wherein the convex regions are not disposed in the first frame area.

6. A method according to claim 1, wherein:

the convex regions are not left in a central area on an inner side of the second frame area; and after the step (e),

the method further comprises steps of:

forming a second interlayer insulating film made of insulating material on the first intra-layer insulating film and the left first film;

forming a via hole through the second interlayer insulating film, the via hole being included in the central area as viewed along a direction parallel to a substrate normal;

forming a second pad on the second interlayer insulating film, the

second pad being connected to the first pad via a region in the via hole; and

wire-bonding a conductive wire to the second pad, a contact area between the conductive wire and the second pad extending to an area on an outer side of the via hole as viewed along a direction parallel to a substrate normal.

7. A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor substrate;

a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part, a plurality of convex regions being left in the pad part, and the recess being formed so that the convex regions are disposed in such a manner that a recess area ratio in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width, becomes larger than a recess area ratio in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width;

a first pad filled in the pad part of the recess; and

a wiring filled in the wiring part of the recess.

8. A semiconductor device according to claim 7, further comprising:

a second interlayer insulating film formed on the first intra-layer

insulating film, the first pad and the wiring, the second interlayer insulating film being formed with at least one via hole, the via hole being disposed partially superposing upon the first pad as viewed along a direction parallel to a substrate normal; and

a second pad formed on the second interlayer insulating film, the second pad being connected to the first pad via a region in the via hole.

9. A semiconductor device according to claim 7, wherein the convex regions are not disposed in the near wiring area.

10. A semiconductor device according to claim 7, wherein the convex regions are not disposed in a central area on an inner side of the second frame area.

11. A semiconductor device according to claim 7, wherein the via hole are included in the first pad as viewed along a direction parallel to a substrate normal.

12. A semiconductor device according to claim 7, wherein the convex regions are disposed regularly in the second frame area along a first direction at a first pitch, and a width of the first frame area along the first direction is equal to or wider than the first pitch.

13. A semiconductor device according to claim 8, further comprising a conductive wire wire-bonded to the second pad, wherein the convex regions are not disposed in a central area on an inner side of the second frame area, the via hole are disposed in the central area, and a contact area between the conductive wire and the second pad extends to an area on an outer side of

the via hole as viewed along a direction parallel to a substrate normal.